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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,208	10/08/2003	Alan J.A. Trainor	027066-001500US	7464

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/680,208	TRAINOR, ALAN J.A.	
	Examiner	Art Unit	
	STANETTA D. ISAAC	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-26 and 33-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-26 and 33-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 April 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment and RCE filed on 8/26/09. Currently, claims 1-7, 9-26 and 33-37 are pending.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/26/09 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-7, 9-26 and 33-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura US Patent (6,734,553, hereinafter referred to as "Kimura") in view of Shi et al (US Patent 7,476,813, hereinafter referred to as "Shi").

5. Kimura discloses the electronic apparatus substantially as claimed. See figures 1A-8, and corresponding text, where Kimura shows, pertaining to claim 1, an electronic apparatus comprising: a first integrated circuit semiconductor die **40** of a first semiconductor technology comprising: a first signal conditioning circuit integrated within the first integrated circuit die for performing a first signal conditioning function on a signal propagating along a first signal path (figures 1A and 1B; col. 4, lines 18-30); a second integrated circuit semiconductor die **50** of a second semiconductor technology physically different from the first semiconductor technology comprising a second signal conditioning circuit integrated within the second integrated circuit semiconductor die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path (figures 1A and 1B; col. 4, lines 18-30); a substrate **10, 20** for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies (figures 1A and 1B; col. 4, lines 30-51).

6. Kimura shows, pertaining to claim 2, wherein the first signal conditioning function and the second signal conditioning function provide similar signal conditioning operations (col. 4, lines 52-67; col. 5, lines 1-5).

7. Kimura shows, pertaining to claim 3, wherein the first semiconductor technology is silicon based technology (col. 4, lines 30-34).

8. Kimura shows, pertaining to claim 4, wherein the second semiconductor technology is other than silicon based technology (col. 4, lines 52-65).

9. Kimura shows, pertaining to claim 5, wherein the first signal conditioning circuit comprises at least a power amplifier circuit and where the function of the first signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit (col. 9, lines 10-15).

10. Kimura shows, pertaining to claim 6, wherein the second signal conditioning circuit comprises at least a power amplifier circuit and where the function of the second signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit (col. 9, lines 10-15).

11. Kimura shows, pertaining to claim 11, wherein the first semiconductor technology is a first one of Si, SiGe, GaAs, InP, and GaN (col. 4, lines 30-32).

12. Kimura shows, pertaining to claim 12, wherein the second semiconductor technology is a second one of Si, SiGe, GaAs, InP, and GaN (col. 4, lines 30-32).

13. Kimura shows, pertaining to claim 13, wherein the first integrated circuit semiconductor die is comprises BiCMOS technology (col. 1, lines 5-22).

14. Kimura shows, pertaining to claim 14, wherein the first integrated circuit die comprises SiGe (col. 5, lines 25-29) .

15. Kimura shows, pertaining to claim 15, wherein the first integrated circuit semiconductor die comprises a first interface port and wherein the second integrated circuit die comprises a second interface port connected to the second signal conditioning circuit, the second signal

conditioning circuit for being connected to the first and second interface ports (figures 1A and 1B).

16. Kimura shows, pertaining to claim 16, wherein the second signal conditioning circuit is for performing the second signal conditioning function in conjunction with operation (figure 1A and 1B).

17. Kimura shows, pertaining to claim 17, an electronic apparatus comprising: a first integrated circuit die formed using a first semiconductor process, the first integrated circuit die **40** of a first semiconductor technology other than requiring additional circuitry for use in performing a first signal conditioning function comprising: a first signal conditioning circuit for performing the first signal conditioning function and having a first input port for receiving a first input signal for performing the first signal conditioning function thereon and having a first output port for providing a first output signal therefrom (figures 1A and 1B; col. 4, lines 18-30); and, a second integrated circuit die **50** of a second semiconductor technology physically different from the first semiconductor technology formed using a second semiconductor process and having a second input port for receiving a second input signal, and a second output port for providing a second output signal therefrom, the second integrated circuit die having a second interface port for interfacing with the first interface port for performing a second signal conditioning function in conjunction with the first integrated circuit die with no signal communication occurring between the first and second input ports and between the first and second output ports (figures 1A and 1B; col. 4, lines 18-30).

18. Kimura shows, pertaining to claim 19, wherein the first signal conditioning function and the second signal conditioning function provide similar signal conditioning operations col. 4, lines 52-67; col. 5, lines 1-5).

19. Kimura shows, pertaining to claim 20, wherein the first semiconductor technology is a silicon based technology (col. 4, lines 30-34).

20. Kimura shows, pertaining to claim 21, wherein the second semiconductor technology is other than silicon based technology (col. 4, lines 52-65).

21. Kimura shows, pertaining to claim 22, wherein the first signal conditioning circuit comprises at least a power amplifier circuit and where the function of the first signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit (col. 9, lines 10-15).

22. Kimura shows, pertaining to claim 24, wherein the first semiconductor technology is one of Si, SiGe, GaAs, InP, and GaN (col. 4, lines 30-32).

23. Kimura shows, pertaining to claim 25, wherein the first integrated circuit die comprises BiCMOS process (col. 1, lines 5-22).

24. Kimura shows, pertaining to claim 26, comprising a module substrate for supporting the first and second integrated circuit dies and for providing electrical connection to and from the first and second integrated circuit dies (figures 1A and 1B; col. 4, lines 30-51).

25. However, Kimura fails to show, pertaining to claims 1 and 17, a first ancillary circuit integrated within the first integrated circuit die and electrically coupled to the first signal conditioning circuit for other than performing the first signal conditioning function and for use by the first signal conditioning circuit during operation thereof; a second ancillary circuit

integrated within the first integrated circuit semiconductor die and electrically coupled to the second signal conditioning circuit for other than performing the second signal conditioning function and for use by the second signal conditioning circuit during operation thereof. In addition, Kimura fails to shows pertaining to claim 7, wherein the second semiconductor technology is less suitable thatn the first semiconductor technology for the integration of an ancillary circuit therein for performing a functionality of the second ancillary circuit. Also, Kimura fails to show, pertaining to claim 9, wherein the first ancillary circuit comprises at least one of voltage regulation circuitry and temperature control circuitry. Kimura fails to show, pertaining to claim 10, wherein the second ancillary circuit comprises at least one of voltage regulation circuitry and temperature control circuitry. In addition, Kimura fails to show, pertaining to claim 17, a first ancillary circuit electrically coupled to the first signal conditioning circuit for use by the first signal conditioning circuit during operation thereof; a second ancillary circuit having a first interface port. Also, Kimura fails to show, pertaining to claim 18, wherein the second integrated circuit die cannot provide the second function without operation of the second ancillary circuit. Kimura fails to show, pertaining to claim 23, wherein the first ancillary circuit and the second ancillary circuit each comprises at least one of voltage regulation circuitry and temperature control circuitry. In addition, Kimura fails to show, pertaining to claim 33, wherein the second semiconductor technology is incompatible for the integration of an ancillary circuit therein for performing the functionality of the second ancillary circuit. Also, Kimura fails to show, pertaining to claim 34, wherein the second semiconductor technology is more costly than the first semiconductor technology for the integration of an ancillary circuit therein for performing the functionality of the second ancillary circuit. Kimura fails to show, pertaining to

claim 35, wherein the second semiconductor technology is less suitable than the first semiconductor technology for the integration of an ancillary circuit therein for performing a functionality of the second ancillary circuit. In addition, Kimura fails to show, pertaining to claim 36, wherein the second semiconductor technology is incompatible for the integration of an ancillary circuit therein for performing the functionality of the second ancillary circuit. Finally, Kimura fails to show, pertaining to claim 37, wherein the second semiconductor technology is more costly than the first semiconductor technology of the integration of an ancillary circuit therein for performing the functionality of the second ancillary circuit.

26. Shi teaches, pertaining to claims 1, 7, 9, 10, 17, 18, 23 and 33-37, a multilayer flip-chip IC die package that includes various ancillary circuits (figure 1; col. 3, lines 25-40). In addition, Shi provides the advantages of achieving desirable impedances (col. 3, lines 1-5).

27. Therefore, it would have been obvious to one of ordinary skill in the art to substitute the following steps of: a first ancillary circuit integrated within the first integrated circuit die and electrically coupled to the first signal conditioning circuit for other than performing the first signal conditioning function and for use by the first signal conditioning circuit during operation thereof; a second ancillary circuit integrated within the first integrated circuit semiconductor die and electrically coupled to the second signal conditioning circuit for other than performing the second signal conditioning function and for use by the second signal conditioning circuit during operation thereof; wherein the second semiconductor technology is less suitable than the first semiconductor technology for the integration of an ancillary circuit therein for performing a functionality of the second ancillary circuit; wherein the first ancillary circuit comprises at least one of voltage regulation circuitry and temperature control circuitry; wherein the second

ancillary circuit comprises at least one of voltage regulation circuitry and temperature control circuitry; a first ancillary circuit electrically coupled to the first signal conditioning circuit for use by the first signal conditioning circuit during operation thereof; a second ancillary circuit having a first interface port; wherein the second integrated circuit die cannot provide the second function without operation of the second ancillary circuit; wherein the first ancillary circuit and the second ancillary circuit each comprises at least one of voltage regulation circuitry and temperature control circuitry; wherein the second semiconductor technology is incompatible for the integration of an ancillary circuit therein for performing the functionality of the second ancillary circuit; wherein the second semiconductor technology is more costly than the first semiconductor technology for the integration of an ancillary circuit therein for performing the functionality of the second ancillary circuit; wherein the second semiconductor technology is less suitable than the first semiconductor technology for the integration of an ancillary circuit therein for performing a functionality of the second ancillary circuit; wherein the second semiconductor technology is incompatible for the integration of an ancillary circuit therein for performing the functionality of the second ancillary circuit; wherein the second semiconductor technology is more costly than the first semiconductor technology of the integration of an ancillary circuit therein for performing the functionality of the second ancillary circuit, in the method of Kimura, pertaining to claims 1, 7, 9, 10, 17, 18, 23 and 33-37, according to the teachings of Shi, with the motivation of achieving desirable impedances allowing for a more efficient semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STANETTA D. ISAAC whose telephone number is (571)272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
September 13, 2009

/Charles D. Garber/
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